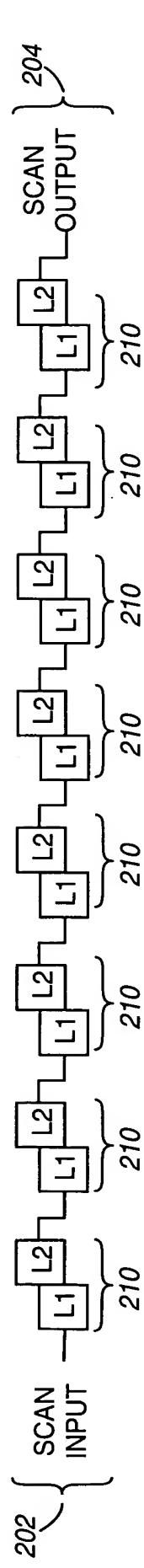
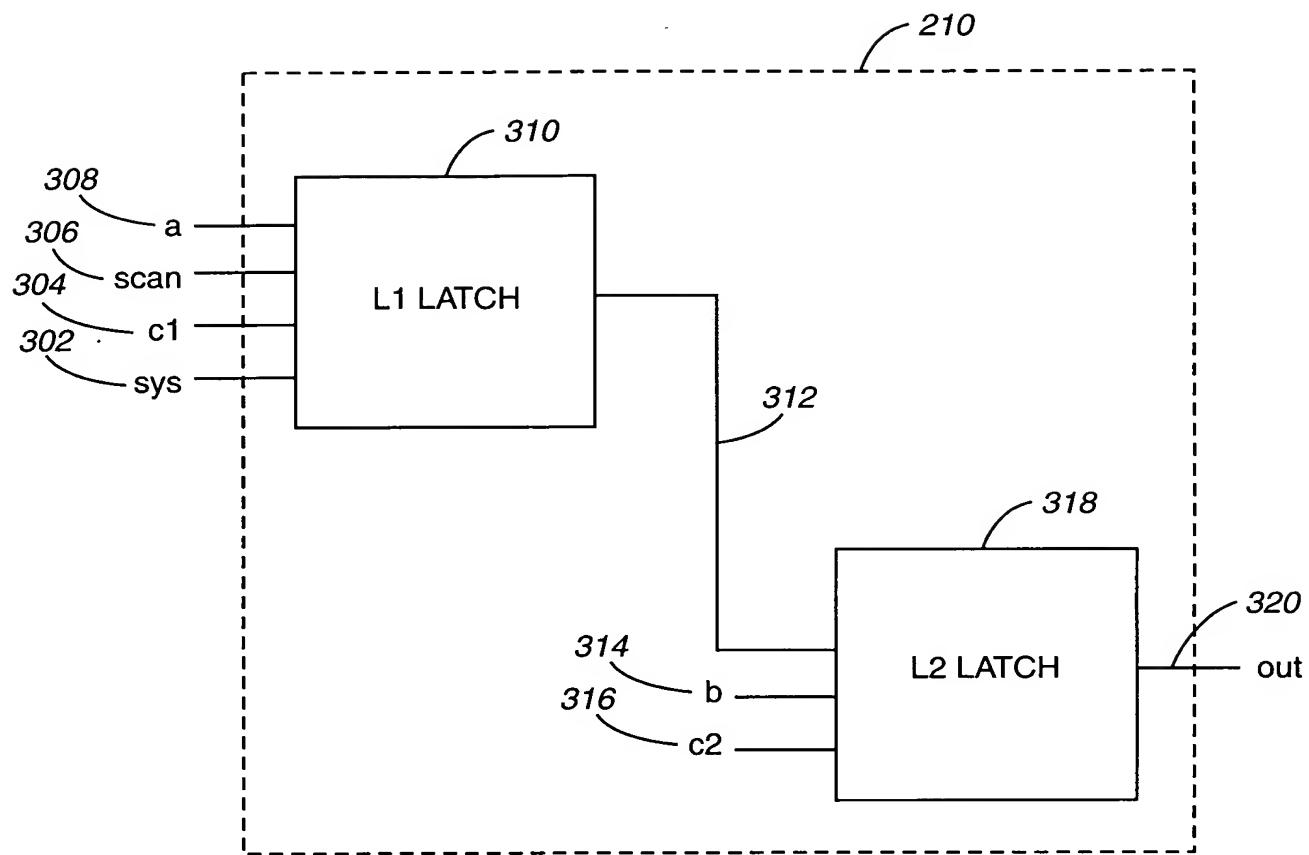


**FIG. 1** PRIOR ART



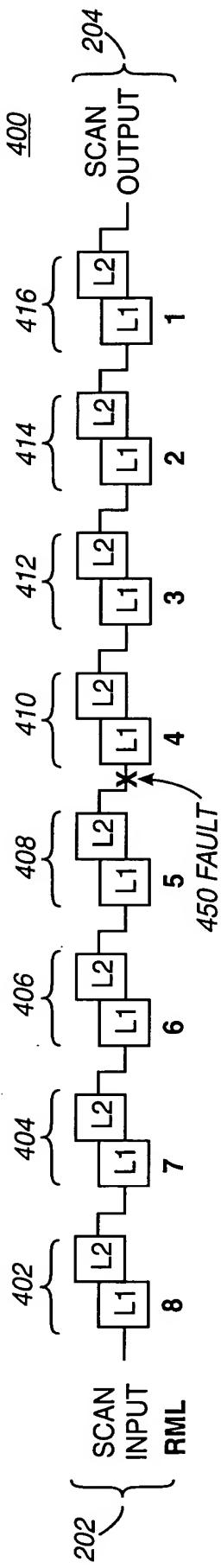
**FIG. 2** PRIOR ART



PRIOR ART

**FIG. 3**





CYCLE

LOAD ALL  
ZERO'S IN  
OPERATING  
REGION

	0	1	2	3	4	5	6	7	8
?	?	?	?	?	?	?	?	?	?
0	?	?	?	?	?	?	?	?	?
0	0	?	?	?	?	?	?	?	?
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

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CYCLE

UNLOAD IN  
FAILING  
REGION

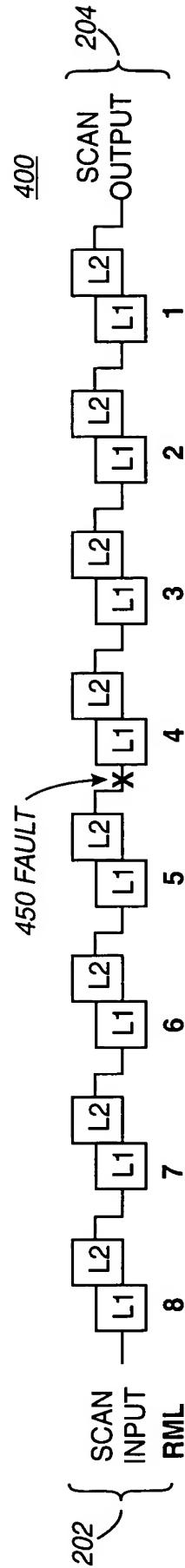
	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

PRIOR ART

FIG. 4



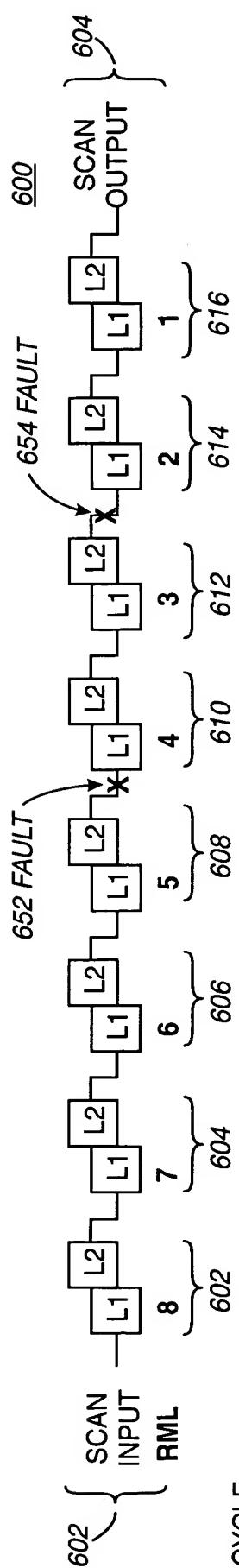


LOAD ALL ZERO'S IN FAILING REGION								
CYCLE	?	?	?	?	?	?	?	?
0	?	?	?	?	?	?	?	?
1	0	?	?	?	?	?	?	?
2	0	0	?	?	?	?	?	?
<u>520</u>	<u>0</u>	<u>0</u>	<u>?</u>	<u>?</u>	<u>?</u>	<u>?</u>	<u>?</u>	<u>?</u>
4	0	0	0	0	?	?	?	?
5	0	0	0	0	1	?	?	?
6	0	0	0	0	1	1	?	?
7	0	0	0	0	1	1	1	?
8	0	0	0	0	1	1	1	1

UNLOAD IN OPERATING REGION								
CYCLE	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	1	1
1	0	0	0	0	0	0	1	1
2	0	0	0	0	0	0	0	1
<u>522</u>	<u>0</u>	<u>1</u>						
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0

**FIG. 5**

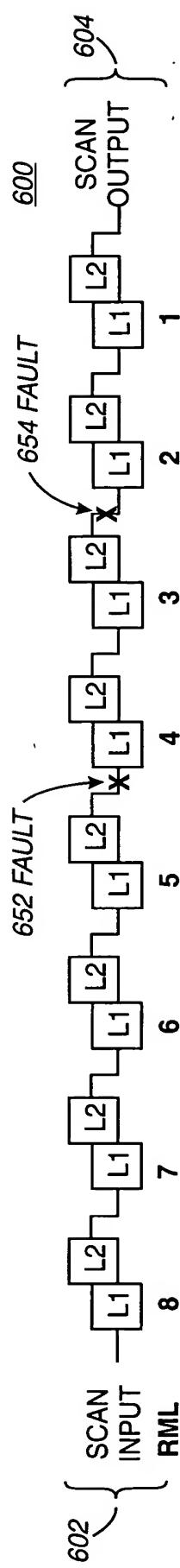




CYCLE	LOAD ALL ZERO'S IN FAILING REGION							
	600	601	602	603	604	605	606	607
0	?	?	?	?	?	?	?	?
1	0	?	?	?	?	?	?	?
2	0	0	?	?	?	?	?	?
3	0	0	0	?	?	?	?	?
4	0	0	0	0	?	?	?	?
5	0	0	0	0	0	?	?	?
6	0	0	0	0	0	0	?	?
7	0	0	0	0	0	0	0	?
8	0	0	0	0	0	0	0	0

CYCLE	UNLOAD IN OPERATING REGION							
	600	601	602	603	604	605	606	607
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0	0
2	0	0	0	0	1	1	1	1
3	0	0	0	0	1	1	1	1
4	0	0	0	0	1	1	1	1
5	0	0	0	0	1	1	1	1
6	0	0	0	0	1	1	1	1
7	0	0	0	0	1	1	1	1

**FIG. 6**



CYCLE

LOAD ALL  
ZERO'S IN  
FAILING  
REGION

	?	?	?	?	?	?	?	?
0	0	?	?	?	?	?	?	?
1	0	0	?	?	?	?	?	?
2	0	0	0	?	?	?	?	?
<u>720</u>	<u>0</u>							
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0

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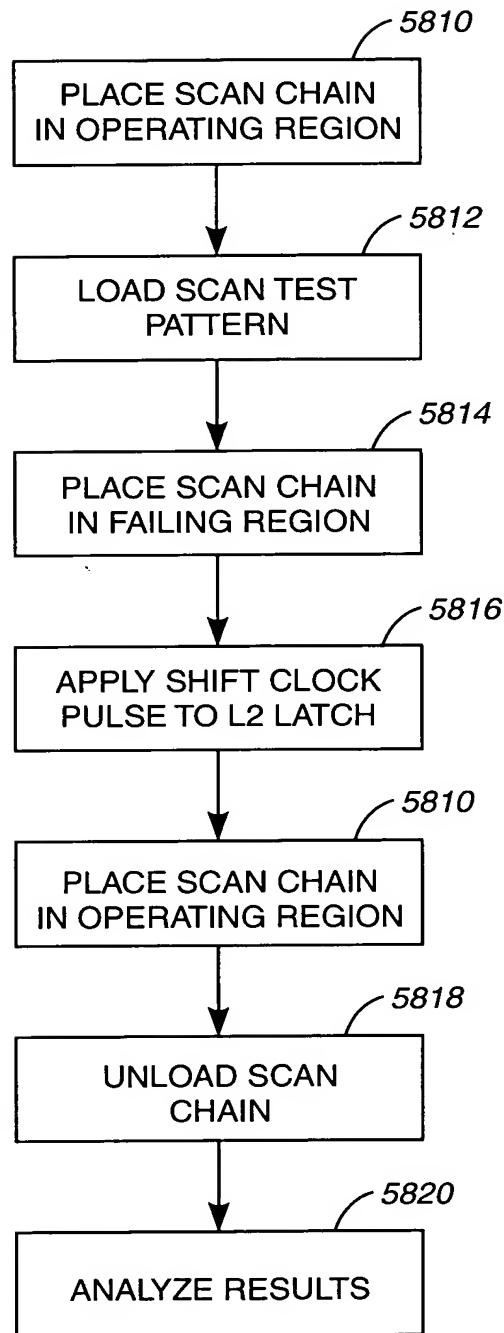
CYCLE

UNLOAD IN  
OPERATING  
REGION

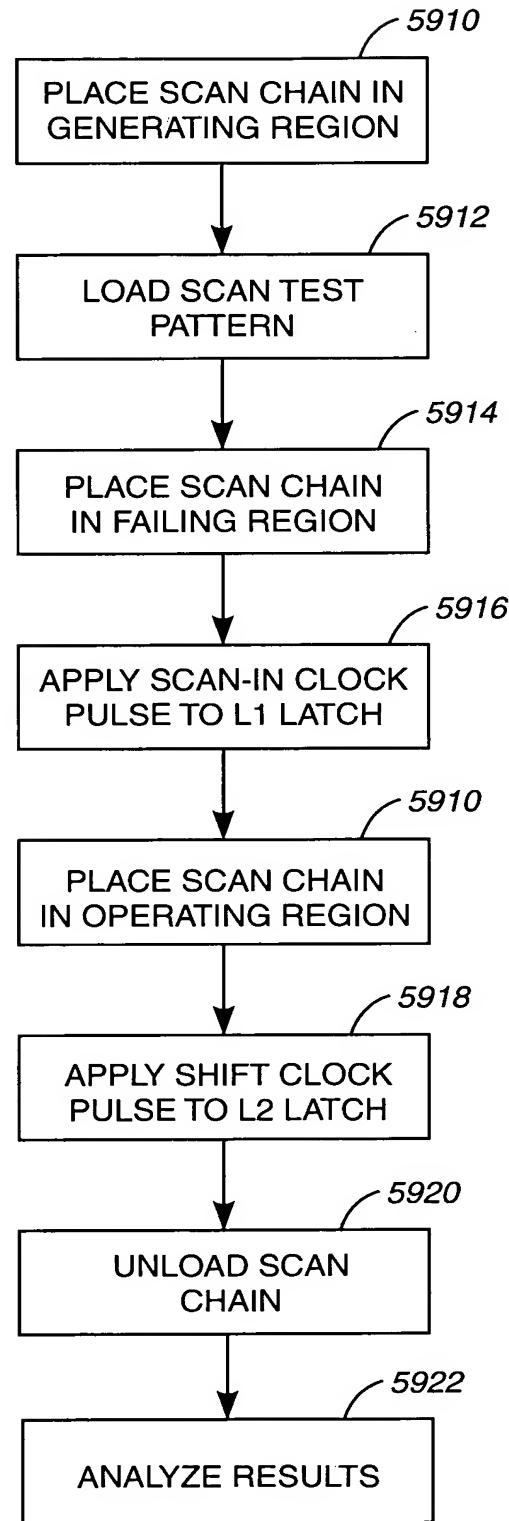
	0	0	0	0	1	1	1
1	0	0	0	0	1	1	1
2	0	0	0	0	0	1	1
<u>722</u>	<u>0</u>	<u>0</u>	<u>0</u>	<u>0</u>	<u>0</u>	<u>0</u>	<u>1</u>
4	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0

PRIOR ART  
**FIG. 7**



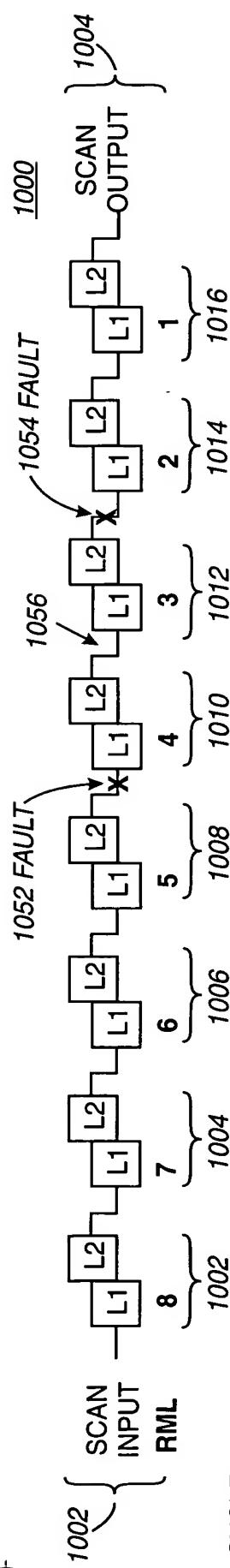


**FIG. 8**



**FIG. 9**





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APPLY SCAN  
CLOCK A  
(SCANNING  
CLOCK) IN  
FAILING REG

## UNLOAD IN OPERATING REGION

## PRIOR ART

FIG. 10

1024 1



INPUT	RML8	RML7	RML6	RML5	RML4	RML3	RML2	RML1		
	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2
1120 LOAD L1 AND L2 WITH ZEROS	0	0	0	0	0	0	0	0	0	0
1122 SWITCH TO FAILING REGION	0	0	0	0	0	1	0	1	0	0
1124 CLOCK A	0	0	0	0	0	1	1	1	1	0
1126 SWITCH TO OPERATING REGION	0	0	0	0	0	1	0	1	0	0
1128 CLOCK B	0	0	0	0	0	0	1	1	1	0
1130 UNLOAD L2	0	0	0	0	0	1	1	1	1	0

**FIG. 11**  
1100





INPUT	RML8	RML7	RML6	RML5	RML4	RML3	RML2	RML1
	L1	L2	L1	L2	L1	L2	L1	L2
LOAD L1 AND L2 WITH ZERO'S	0	0	0	0	0	0	0	0
1220								
SWITCH TO FAILING REGION	0	0	0	0	1	0	1	0
1222								
CLOCK B	0	0	0	0	1	1	1	0
1224								
SWITCH TO OPERATING REGION	0	0	0	0	0	1	0	0
1226								
UNLOAD L2	0	0	0	0	1	1	1	0
1228								

**FIG. 12**  
1200

